539,333

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 July 2004 (15.07.2004)

PCT

(10) International Publication Number
WO 2004/059726 A1

(51) International Patent Classification[7]: H01L 21/82, 21/44

(21) International Application Number: PCT/US2002/041182

(22) International Filing Date: 20 December 2002 (20.12.2002)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,

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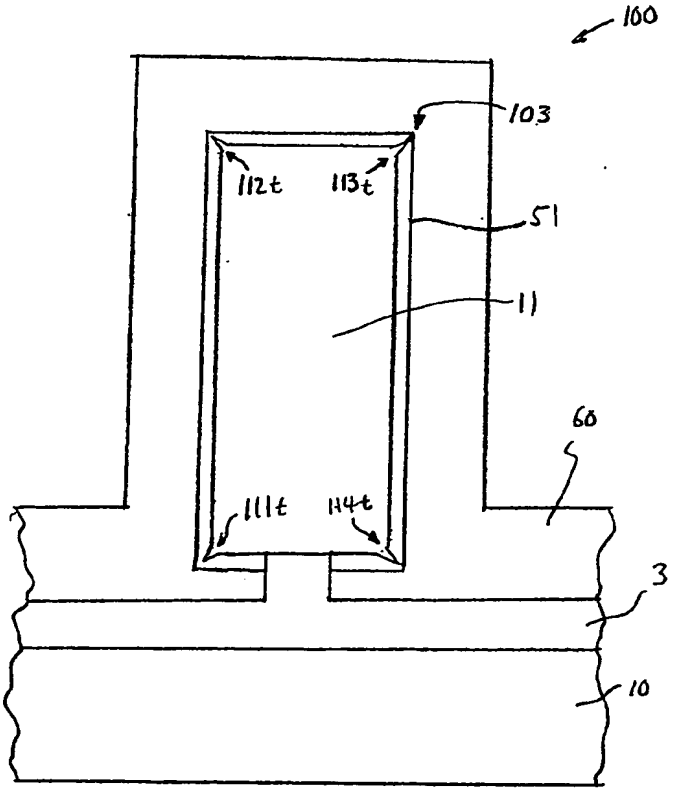
(54) Title: INTEGRATED ANTIFUSE STRUCTURE FOR FINFET AND CMOS DEVICES



(57) Abstract: A method is described for fabricating and antifuse structure (100) integrated with a semiconductor device such as a FINFET or planar CMOS devise. A region of semiconducting material (11) is provided overlying an insulator (3) disposed on a substrate (10); an etching process exposes a plurality of corners (111-114) in the semiconducting material. The exposed corners are oxidized to form elongated tips (111t-114t) at the corners; the oxide (31) overlying the tips is removed. An oxide layer (51), such as a gate oxide, is then formed on the semiconducting material and overlying the corners; this layer has a reduced thickness at the corners. A layer of conducting material (60) is formed in contact with the oxide layer (51) at the corners, thereby forming a plurality of possible breakdown paths between the semiconducting material and the layer of conducting material through the oxide layer. Applying a voltage, such as a burn-in voltage, to the structure converts at least one of the breakdown paths to a conducting path (103, 280).

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MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) **Designated States** *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*

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